Amendments to the Claims:

This listing of claims will replace all prior version, and listings, of claims in the application:

Listing of Claims:

1 (currently amended): A method comprising:

analyzing characteristics of signals passing along a first plurality of conductive paths arranged in a first ~~orientation~~ arrangement;

determining a second ~~orientation~~ arrangement for a second plurality of conductive paths based on said analyzed characteristics, the second arrangement effecting a rearrangement of the first plurality of conductive paths; and

designing ~~the~~ a structure having the first plurality of conductive paths arranged in the first ~~orientation~~ arrangement and the second plurality of conductive paths in the determined second ~~orientation~~ arrangement.

2 (original): The method of claim 1, wherein said characteristics comprise timing relationships of signals across said first plurality of conductive paths.

3 (original): The method of claim 2, wherein said timing relationships relate to one of push-out and pull-in of signal timings.

4 (currently amended): The method of claim 1, wherein said first plurality of conductive paths are on a first plane and arranged in said first ~~orientation~~ arrangement and said second plurality of conductive paths are on a second plane and arranged in said second ~~orientation~~ arrangement.

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5 (original): The method of claim 1, wherein said first plurality of conductive paths comprise a first plurality of traces on a first layer of a printed circuit board and said second plurality of conductive paths comprise a second plurality of traces on a second layer of said printed circuit board.

6 (currently amended): The method of claim 5, wherein said first plurality of traces are arranged on said first layer in a first ~~ordered arrangement~~ order and said second plurality of traces are arranged on said second layer in a second ~~ordered arrangement~~ order and determining said second ~~orientation~~ arrangement comprises determining said second ~~ordered arrangement~~ order based on the analyzed characteristics.

7 (original): The method of claim 1, wherein said first plurality of conductive paths comprise a first plurality of vias coupling a first layer of a printed circuit board to a second layer of said printed circuit board, and said second plurality of conductive paths comprise a second plurality of vias coupling said first layer of said printed circuit board to said second layer of said printed circuit board.

8 (currently amended): A method of designing a printed circuit board comprising:

analyzing at least one characteristic of a first plurality of relatively parallel conductive paths on said printed circuit board, said first plurality of relatively parallel conductive paths being arranged in a pattern in a first area of said printed circuit board;

rearranging said pattern of conductive paths based on the analyzed at least one characteristic such that at least a portion of at least one of a second plurality of relatively parallel conductive paths in a second area of said printed circuit board ~~have a different geometry with respect to one another as compared~~

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~~to a geometry~~ is laterally offset with respect to a corresponding path of said first plurality of relatively parallel conductive paths in said first area; and

designing the printed circuit board having the first plurality of relatively parallel conductive paths and the second plurality of relatively parallel conductive paths.

9 (canceled)

10 (original): The method of claim 8, wherein said at least one characteristic comprises a timing relationship of signals along said first plurality of relatively parallel conductive paths.

11 (original): The method of claim 10, wherein said timing relationship relates to one of push-out and pull-in of signal timings.

12 (currently amended): The method of claim 8, wherein said first plurality of relatively parallel conductive paths are on a first layer of said printed circuit board and said second plurality of relatively parallel conductive paths are on a second ~~plane~~ layer of said printed circuit board.

13 (original): The method of claim 8, wherein said first plurality of relatively parallel conductive paths comprise a first plurality of traces on a first layer of said printed circuit board and said second plurality of relatively parallel conductive paths comprise a second plurality of traces on a second layer of said printed circuit board.

14 (original): The method of claim 13, wherein said first plurality of traces are arranged on said first layer in a first ordered arrangement and said second plurality of traces are arranged on said second layer in a second ordered

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arrangement, and rearranging said pattern comprises determining said second ordered arrangement based on said analyzed at least one characteristic.

15 (original): The method of claim 8, wherein said first plurality of relatively parallel conductive paths comprise a first plurality of vias coupling a first layer of said printed circuit board to a second layer of said printed circuit board, and said second plurality of conductive paths comprise a second plurality of vias coupling said first layer of said printed circuit board to said second layer of said printed circuit board.

16 (currently amended) : A method comprising:
   analyzing a characteristic of a first plurality of conductive paths arranged in a first pattern;
   altering said characteristic by rearranging said pattern to form a second pattern; and
   designing a structure to have said first pattern and said second pattern;
   wherein altering said characteristic comprises determining the second pattern for a second plurality of conductive paths based on said analyzed characteristic, the second pattern effecting a rearrangement of the first plurality of conductive paths.

17 (original): The method of claim 16, wherein said characteristic comprises a timing relationship of signals across said first plurality of conductive paths.

18 (original): The method of claim 17, wherein said timing relationship relates to one of push-out and pull-out of signal timings.

19 (canceled)

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20 (currently amended):The method of claim 49 16, wherein said first plurality of conductive paths are on a first plane and arranged in said first pattern and said second plurality of conductive paths are on a second plane and arranged in said second pattern.

21 (currently amended): The method of claim 49 16, wherein said first plurality of conductive paths comprise a first plurality of traces on a first layer of a printed circuit board and said second plurality of conductive paths comprise a second plurality of traces on a second layer of said printed circuit board.

22 (canceled)

23 (currently amended): The method of claim 49 16, wherein said first plurality of conductive paths comprise a first plurality of vias coupling a first layer of a printed circuit board to a second layer of said printed circuit board, and said second plurality of conductive paths comprise a second plurality of vias coupling said first layer of said printed circuit board to said second layer of said printed circuit board.

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